What is claimed is:

1. A method usable with a memory device, comprising:

receiving a data strobe signal from a memory bus;

capturing data associated with a write command from the memory bus in synchronization with the data strobe signal;

performing a column redundancy check in response to an address associated with the write command; and

synchronizing the beginning of an internal write operation to a memory cell array of the memory device to a clock signal.

2. The method of claim 1, wherein the internal write operation begins on an edge of the clock signal.

3. The method of claim 1, further comprising:

providing the column select signals to the memory cell array in synchronization with the clock signal.

4. The method of claim 3, wherein the providing the column select signals comprises:

latching the column select signals synchronously with an edge of a clock signal.

5. The method of claim 4, wherein the latching the column select signals comprises asserting a column address trap signal synchronously with the edge of the clock signal.

6. The method of claim 1, wherein the column redundancy check is performed beginning on a first edge of a clock signal and the providing the column select signals begins on another edge of the clock signal.

7. The method of claim 1, wherein the synchronization of the internal write operation to the clock signal establishes time for equalization of input/output lines before the beginning of a successive internal read operation.

8. A method usable with a memory device, comprising:

receiving first signals indicative of an address associated with a write command;

latching data associated with the write command in response to a data strobe signal;

decoding the address to produce a column address;

providing column select signals indicative of the column address to a memory cell array of the memory device;

delaying initiation of the providing of the column select signals to accommodate variation in a timing of the data strobe signal; and

performing a column redundancy check prior to the initiation of the providing of the column select signals.

9. The method of claim 8, wherein the providing the column select signals comprises latching the column select signals synchronously with an edge of a clock signal.

10. The method of claim 9, wherein the latching the column select signals comprises asserting a column address trap signal synchronously with the edge of the clock signal.

11. The method of claim 8, wherein the performing the column redundancy check begins on a first edge of a clock signal and the providing the column select signals begins on another edge of the clock signal.

12. The method of claim 11, wherein said another edge comprises the next successive edge of the clock signal after the first edge.

13. The method of claim 8, further comprising:

asserting another signal to equalize a data I/O line for a first time interval that begins after the providing the column select signals.

14. The method of claim 13, further comprising:

deasserting said another signal to terminate the first time interval; and

beginning an internal read operation after the deassertion of said another signal.

15. The method of claim 13, further comprising:

asserting said another signal after the read operation for a second time interval less than the first time interval.

16. The method of claim 8, wherein the memory device comprises a double data rate synchronous dynamic random access memory.

17. A memory device comprising:

a memory cell array;

a data communication circuit to receive a data strobe signal from a memory bus and capture data associated with a write command from the memory bus in synchronization with the data strobe signal;

an addressing circuit to generate a decoded address in response to address signals provided from the memory bus and perform a column redundancy check in response to the decoded address; and

a control circuit to synchronize the initiation of an internal write operation to the memory cell array with a clock signal.

18. The memory device of claim 17, wherein the control circuit synchronizes the initiation of the internal write operation to an edge of the clock signal.

19. The memory device of claim 17, wherein the addressing circuit further provides column select signals to the memory cell array in synchronization with the clock signal.

20. The memory device of claim 19, wherein the addressing circuit latches the column select signals synchronously with an edge of the clock signal.

21. The memory device of claim 20, wherein the control circuit pulses a column address trap signal synchronously with an edge of the clock signal, and the addressing circuit latches the column select signals in response to a pulse of the column address trap signal.

22, The memory device of claim 17, wherein the addressing circuit performs the column redundancy check beginning on a first edge of a clock signal and provides the column select signals beginning on another edge of the clock signal.

23. A memory device comprising:

a memory cell array;

an addressing circuit to receive first signals indicative of an address associated with a write command, decode the address to provide column select signals to the memory cell array indicative of a column address in the memory cell array and use the column address to perform a column redundancy check;

a data communication circuit to latch data signals associated with the write command in response to a data strobe signal; and

a control circuit to cause the addressing circuit to perform the column redundancy check during a delay to accommodate variations in the timing of the data strobe signal and begin providing the column select signals to the memory cell array after performing the column redundancy check.

24. The memory device of claim 23, wherein the addressing circuit provides the column select signals by latching the column select signals synchronously with an edge of a clock signal.

25. The memory device of claim 24, wherein the addressing circuit latches the column select signals in response to a column address trap signal, and the control circuit asserts the column address trap signal synchronously with the edge of the clock signal.

26. The memory device of claim 24, wherein the addressing circuit begins performing the column redundancy check on a first edge of a clock signal and begins providing the column select signals begins on another edge of the clock signal.

27. The memory device of claim 26, wherein said another edge comprises the next successive edge of the clock signal after the first edge.

28. The memory device of claim 23, wherein the control circuit asserts another signal to equalize data I/O lines for a first time interval that begins after the addressing circuit provides the column select signals.

29. The memory device of claim 23, wherein the memory device comprises a double data rate synchronous dynamic random access memory.

30. A computer system comprising:

a memory bus;

a memory controller coupled to the memory bus;

a central processing unit to cause the memory controller to furnish signals to the memory bus to cause a write operation, the signals including a data strobe signal; and

a memory device coupled to the memory bus and adapted to:

capture data associated with the write operation in response to the data strobe signal,

establish a predetermined window of time to capture the data, and

perform a column redundancy check in response to the write operation during the predetermined window of time.

31. The computer system of claim 30, wherein

the signals include signals that indicate a write command, and

the memory device is further adapted to capture said signals that indicate the write command in synchronization with a clock signal and begin an internal write operation to a memory cell array of the memory device in synchronization with the clock signal.

32. The computer system of claim 31, wherein the memory device begins performing the column redundancy check on a first edge of a clock signal and begins performing the internal write operation on another edge of the clock signal.

33. The computer system of claim 32, wherein said another edge comprises the next successive edge of the clock signal after the first edge.

34. The computer system of claim 30, wherein the memory device begins the internal write operation in response to a column address trap signal, and the memory device includes a control circuit to assert the column address trap signal synchronously with the edge of the clock signal.

35. The computer system of claim 34, wherein the control circuit asserts another signal to equalize data I/O lines for a first time interval that begins after the memory device begins the internal write operation.

36. The computer system of claim 30, wherein the memory device comprises a double data rate synchronous dynamic random access memory.